United States Patent [19]

Buchanan

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[54] **CHIP TOPOGRAPHY FOR MOS INTEGRATED CIRCUITRY MICROPROCESSOR CHIP**

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[52] **U.S. Cl.** **340/172.5**

[51] **Int. Cl.**[2] **G06F 1/00**

[58] **Field of Search** 340/172.5; 445/1

[56] **References Cited**

UNITED STATES PATENTS

3,579,201	8/1971	Langley	340/172.5
3,716,843	2/1973	Schmitt et al.	340/172.5
3,757,306	9/1973	Boone	340/172.5
3,757,308	9/1973	Fosdick	340/172.5
3,758,761	9/1973	Henrion	235/153 AK
3,760,367	9/1973	Kortenhaus	340/172.5
3,760,369	9/1973	Kemp	340/172.5
3,798,606	3/1974	Henle et al.	340/172.5
3,821,715	6/1974	Hoff et al.	340/172.5
3,832,694	8/1974	Judith	340/172.5
3,896,418	7/1975	Brown	340/172.5
3,906,453	9/1975	Mattedi et al.	340/172.5
3,912,947	10/1975	Buchanan	307/269
3,962,682	6/1976	Bennett	340/172.5

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[57] **ABSTRACT**

The chip architecture of an MOS microprocessor chip includes data bus input-output buffer circuitry located along the lower right hand edge of the chip. High order address buffer output circuitry is located along the bottom of the chip. Directly to the left of the data bus input-output buffer circuitry is the arithmetic logic unit circuitry, and to the right of this and adjacent to the high order address bit buffer circuitry is located a register section including first accumulator register, a second accumulator register, high and low order index registers, a high order incrementer and an associated program counter, a low order incrementer and associated program counter, a high order stack pointer register and a low order stack pointer register, and a temporary register arranged on the surface of the microprocessor chip in a particular sequence. To the left of the register section and along the lower left hand edge of the chip is located a plurality of low order address bit buffer circuits. Above and coupled to the register section and to the arithmetic logic unit is located a plurality of bootstrap driver circuits for driving signals which enable programmed data transfers between the various registers, the arithmetic logic unit and a plurality of internal data bus and address bus conductors coupled to the data bus input-output buffer circuitry and the high order and the low order address bit buffer circuits, respectively. Read/write circuitry, a condition code register, decision logic circuitry, and an instruction register are located in sequence along the upper righthand edge of the chip. To the left of the decision logic circuitry and the condition code register and above the bootstrap driver circuitry and coupled thereto is a logic control circuitry section. Above the logic control circuitry and along the upper edge of the chip to the left of the instruction register is located an instruction decoder circuitry section. Along the upper lefthand edge of the chip is located input-output control circuitry and look-ahead circuitry for the instruction decoder. Between the lefthand portion of the logic control circuitry and the right hand portion of the I/O control circuitry is located timing generator circuitry coupled to the logic control circuitry for enabling the selected logic gates therein, which are selected and driven by the instruction decoder.

9 Claims, 9 Drawing Figures